

Attorney Docket No.: 0180154

**REMARKS**

Prior to the present amendment, claims 1-14 were pending in the present application. By this amendment, Applicant has amended claims 1 and 8, and has canceled claims 3, 7, 10 and 14. Thus, claims 1-2, 4-6, 8-9, and 11-13 remain in the present application. Reconsideration and allowance of pending claims 1-2, 4-6, 8-9, and 11-13 in view of the above amendments and the following remarks are respectfully requested.

The Examiner has rejected claims 1-2, 6, 8-9, and 13 under 35 USC §102(a) as being anticipated by U.S. Patent No. 6,563,183 to En et al (hereinafter "En"). Applicant respectfully submits that the present invention, as defined by amended claims 1 and 8, is patentably distinguishable over En. En is directed to a gate array with multiple dielectric properties. According to En, an integrated circuit is fabricated on a semiconductor substrate, including first and second field effect transistors. The first field effect transistor includes a first polysilicon gate positioned above a first channel region of the substrate and isolated from the first channel region by a first dielectric layer extending the entire length of the first polysilicon gate. The first dielectric layer includes a first dielectric material with a first dielectric constant. The second field effect transistor consists of a second polysilicon gate positioned above a second channel region on the substrate and isolated from the second channel region by a second dielectric layer extending the entire length of the second polysilicon gate. The second dielectric layer has a second dielectric material with a second dielectric constant. The first dielectric constant

Attorney Docket No.: 0180154

and the second dielectric constant may be different. See the flow chart of Figure 2, and Figures 5a through 5i and their related descriptions in En.

According to En, utilization of different dielectrics with different dielectric constants results in a gate array that can include smaller, faster transistors having a high dielectric constant, with additional flexibility in that transistors with different operating properties can be fabricated and used. See, column 10, lines 13-21 of En.

However, En is not directed to formation of a thin, high quality buffer layer in a field effect transistor in order to prevent the problems associated with low quality, non-uniform, thick, lower-k, and pin-holed dielectrics resulting from randomly and unintendedly grown thermal oxide at the silicon/high k interface in a field effect transistor. See, for example, page 8, line 20 through page 9, line 9 of the present application. Thus, the present invention discloses and claims "utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form a buffer layer" on the substrate and "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer being selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide." In addition to the fact that En does not address the problems addressed by the present invention, En does not disclose or suggest, for example, use of silicon tetrachloride precursor, nor use of aluminum oxide as a high-k dielectric. As such, the present invention, as defined by the amended claims, is patentably distinguishable over En.

Attorney Docket No.: 0180154

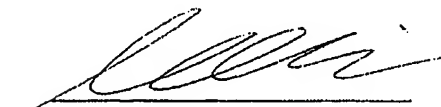
The Examiner has cited U.S. Patent Publication No. 2005/0048765 to Kim (hereinafter "Kim") as disclosing use of silicon tetrachloride to form oxide in an ALD process. However, Kim is directed to sealing pores in a *low-k dielectric* damascene process for forming conductive layers. See, for example, Figure 3A of Kim and its related description. As such, Kim specifically teaches away from use of an ALD layer in conjunction with *high-k dielectrics*. For example, Kim does not disclose or suggest "forming a high-k dielectric layer over [the] buffer layer, [the] high-k dielectric layer being selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide." Moreover, Kim is not directed to fabrication of a field effect transistor or its gate, but to the formation of conductive patterns in a damascene process. As such, Kim does not provide suggestions or teachings to cure the deficiencies of En.

For all the foregoing reasons, Applicant submits that claims 1-2, 4-6, 8-9, and 11-13 remaining in the present application are patentably distinguishable over En and Kim, either singly or in combination. As such, an early notice of allowance directed to pending claims 1-2, 4-6, 8-9, and 11-13 is respectfully requested.

Attorney Docket No.: 0180154

Respectfully Submitted,  
FARJAMI & FARJAMI LLP

Date: 5/13/05

  
Michael Farjami, Esq.  
Reg. No. 38,135

FARJAMI & FARJAMI LLP  
26522 La Alameda Ave., Suite 360  
Mission Viejo, California 92691  
Telephone: (949) 282-1000  
Facsimile: (949) 282-1002

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number 703-872-9306 on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 5/13/05

Christina Carter  
Name of Person Performing Facsimile Transmission

Christina Carter 5/13/05  
Signature Date

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: \_\_\_\_\_

\_\_\_\_\_  
Name of Person Mailing Paper and/or Fee

\_\_\_\_\_  
Signature Date